



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE Technology Center 3600

In re application of:

Brian P. Evans et al.

Serial No.:

09/943,947

Art Unit:

2661

Filed:

August 31, 2001

Examiner:

For:

CONFIGURABLE MATRIX ARCHITECTURE

Assistant Commissioner For Patents Washington, D.C. 20231

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT WITHIN THREE MONTHS OF FILING OR **BEFORE MAILING OF FIRST OFFICE ACTION (37 CFR 1.97(b))**

NOTE: "An information disclosure statement shall be considered by the Office if filed: (1) within three months of the filing date of a national application; (2) within three months of the date of entry of the national stage as set forth in § 1.491 in an international application; or (3) before the mailing date of a first Office action on the merits, whichever event occurs last." 37 CFR 1.97(b).

IDENTIFICATION OF TIME OF FILING THE ACCOMPANYING INFORMATION DISCLOSURE STATEMENT

The information disclosure statement submitted herewith is being filed within three months of the filing date of the application or date of entry into the national stage of an international application before the mailing date of a first Office action on the merits, whichever event occurs last. 37 CFR 1.97(b).

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Dated: October 10, 2001

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on October 10, 2001.

Sheet	1	of	1

Form PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE								TENT AND	ATTY DOCKET NO. 0325.00504	SERIAL NO 09/943,947				
INFORMATION DISCLOSURE									APPLICANT: Brian P. Evans et al.					
STATEMENT BY APPLICANT								\	FILING DATE August 31, 2001	GROUP 2661				
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					ОТ	HE	R	DOCUMENTS	(Incl. Author, Title, Date, Per	rtinent Pages, etc.)				
	Benjamin J. Bowers et al., "PUSH/PULL MULTIPLEXER BIT", U.S. Serial No. 09/940,406, Filed August 27, 2001.													
	Brian P. Evans et al., "LAYOUT ARCHITECTURE TO OPTIMIZE PATH DELAYS", U.S. Serial No. 09/941,352, Filed August 29, 2001.													
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